

FIG. 1
PRIOR ART



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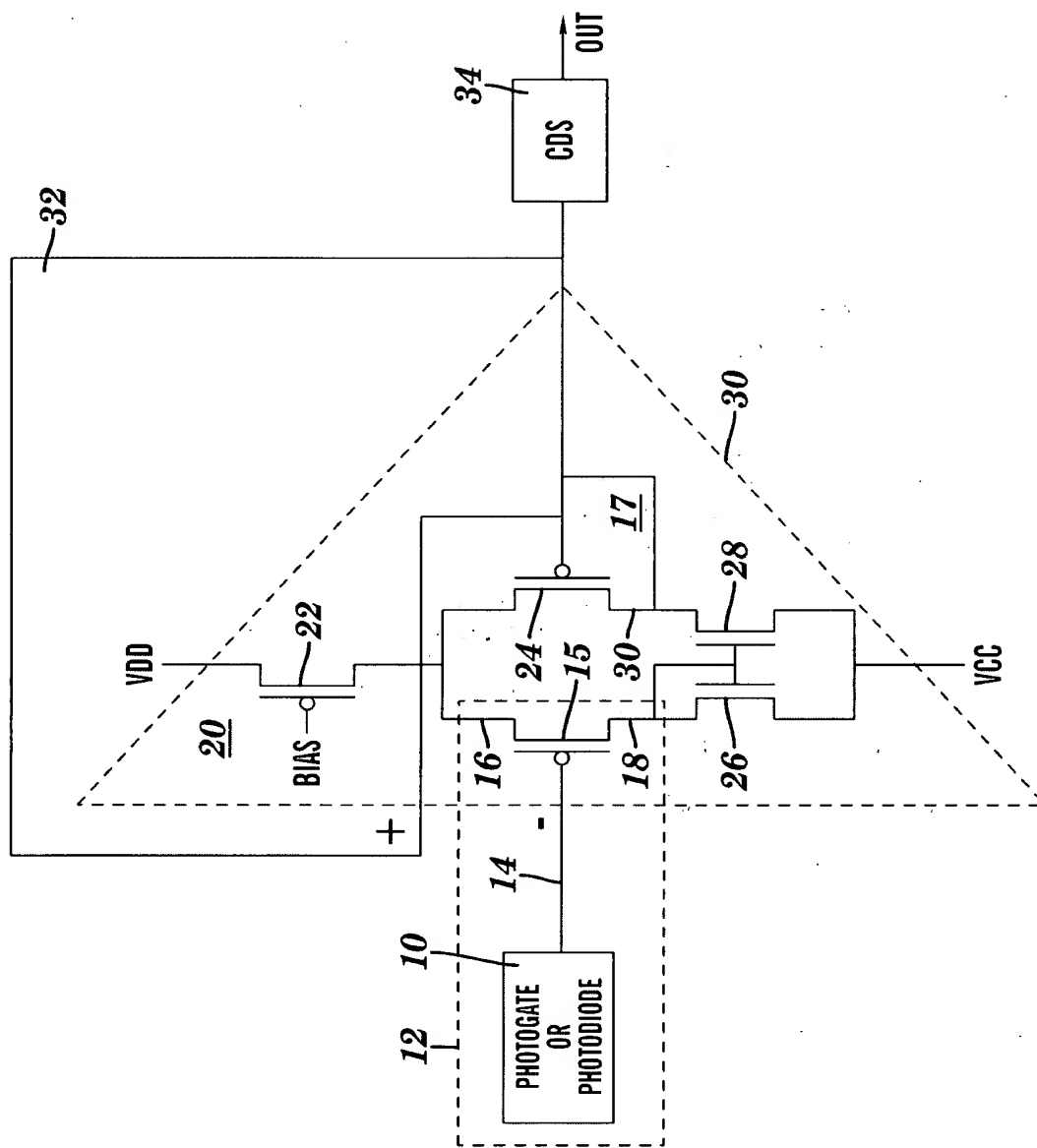


FIG. 2

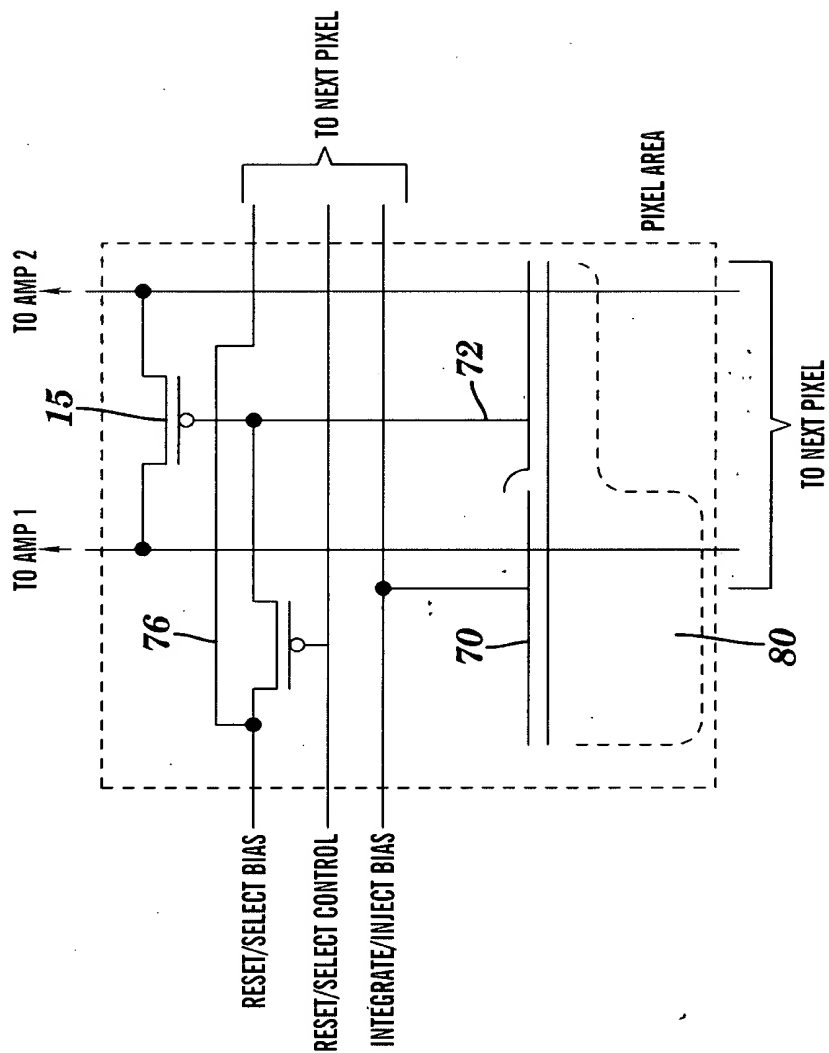


FIG. 3



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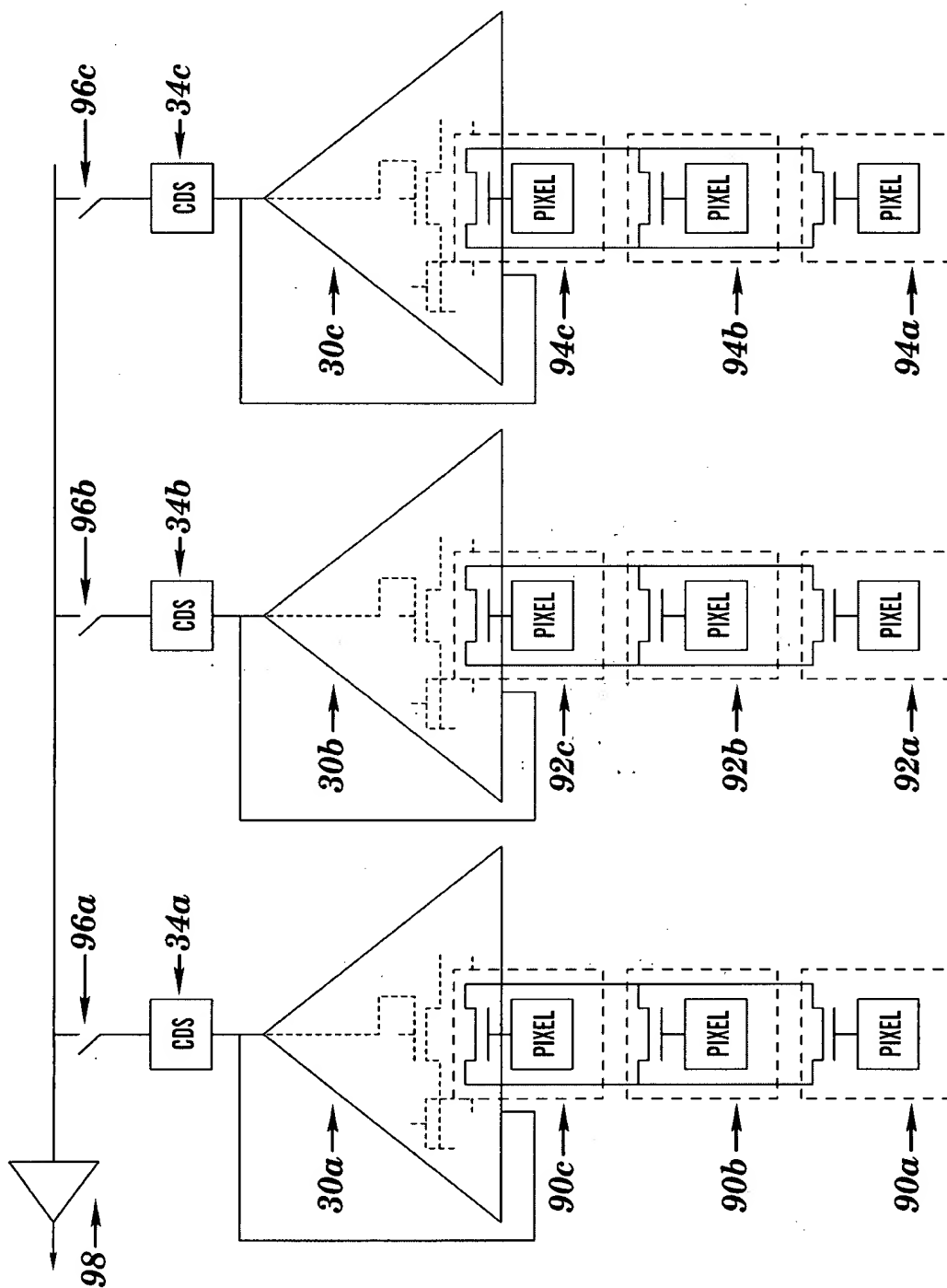


FIG. 4



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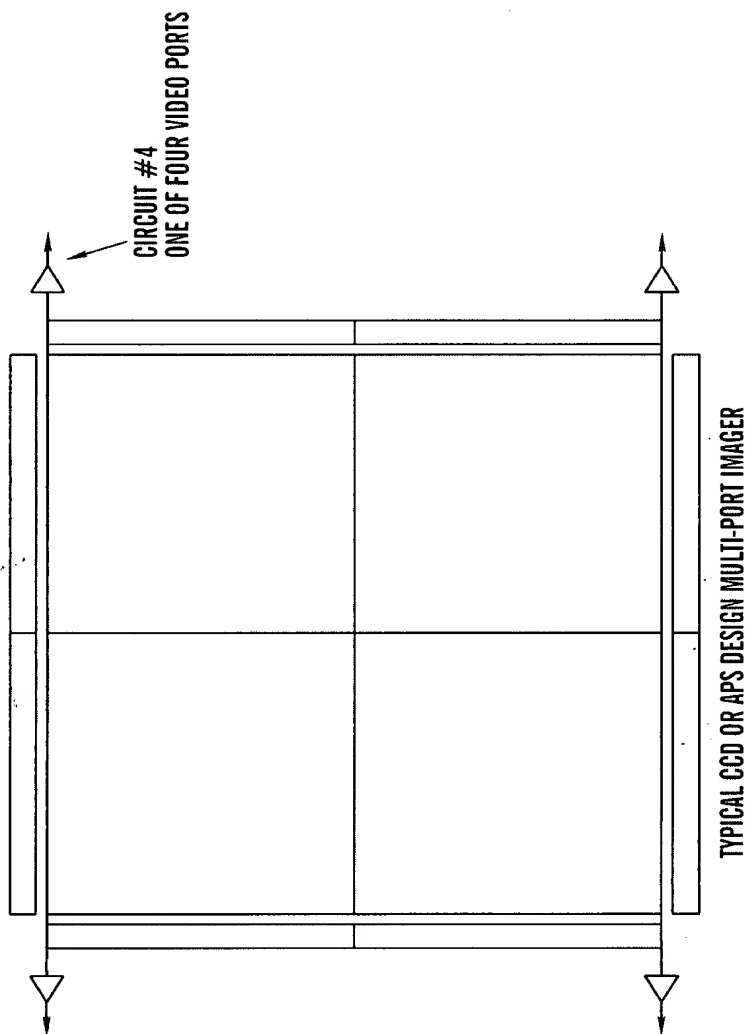


FIG. 5

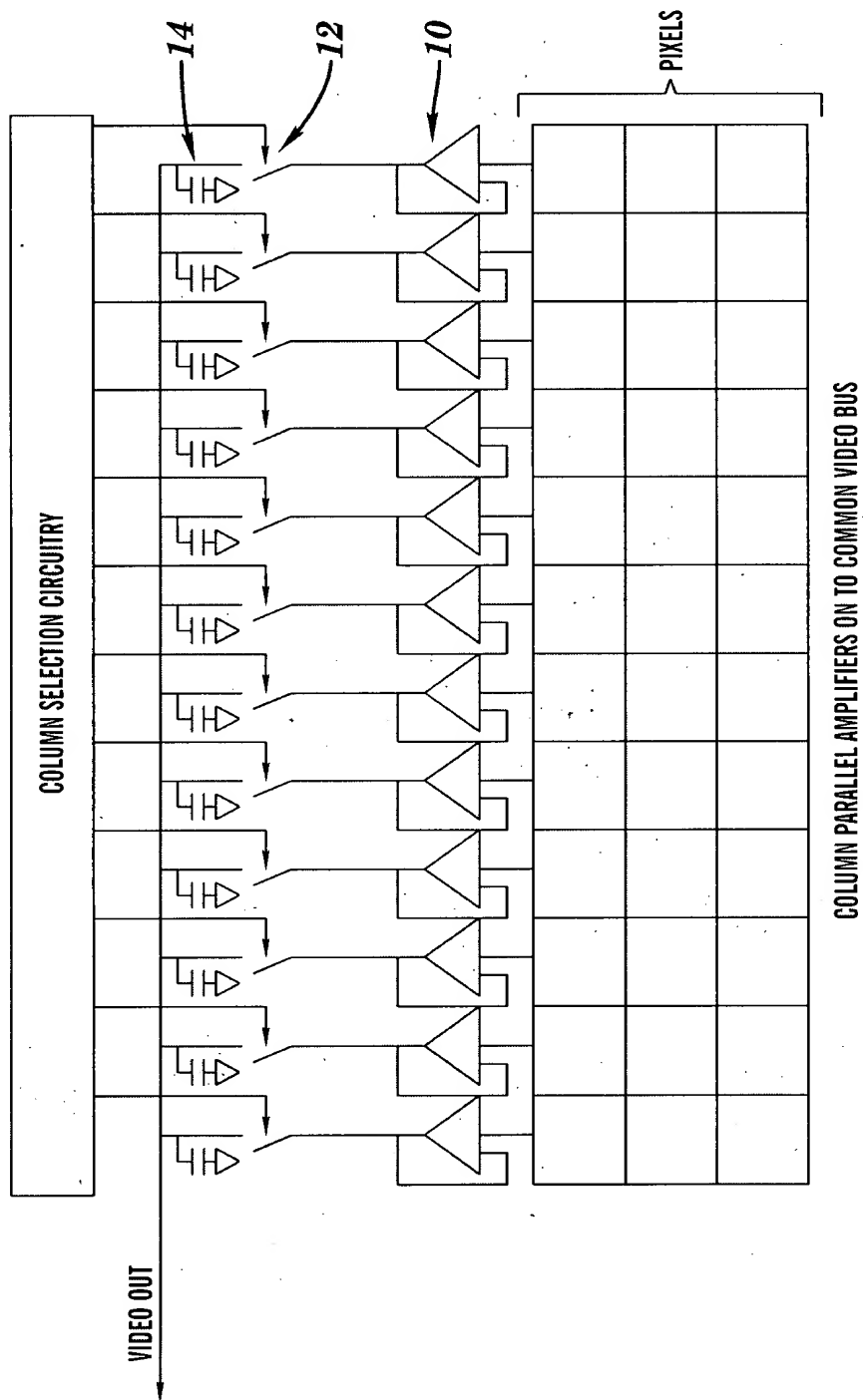
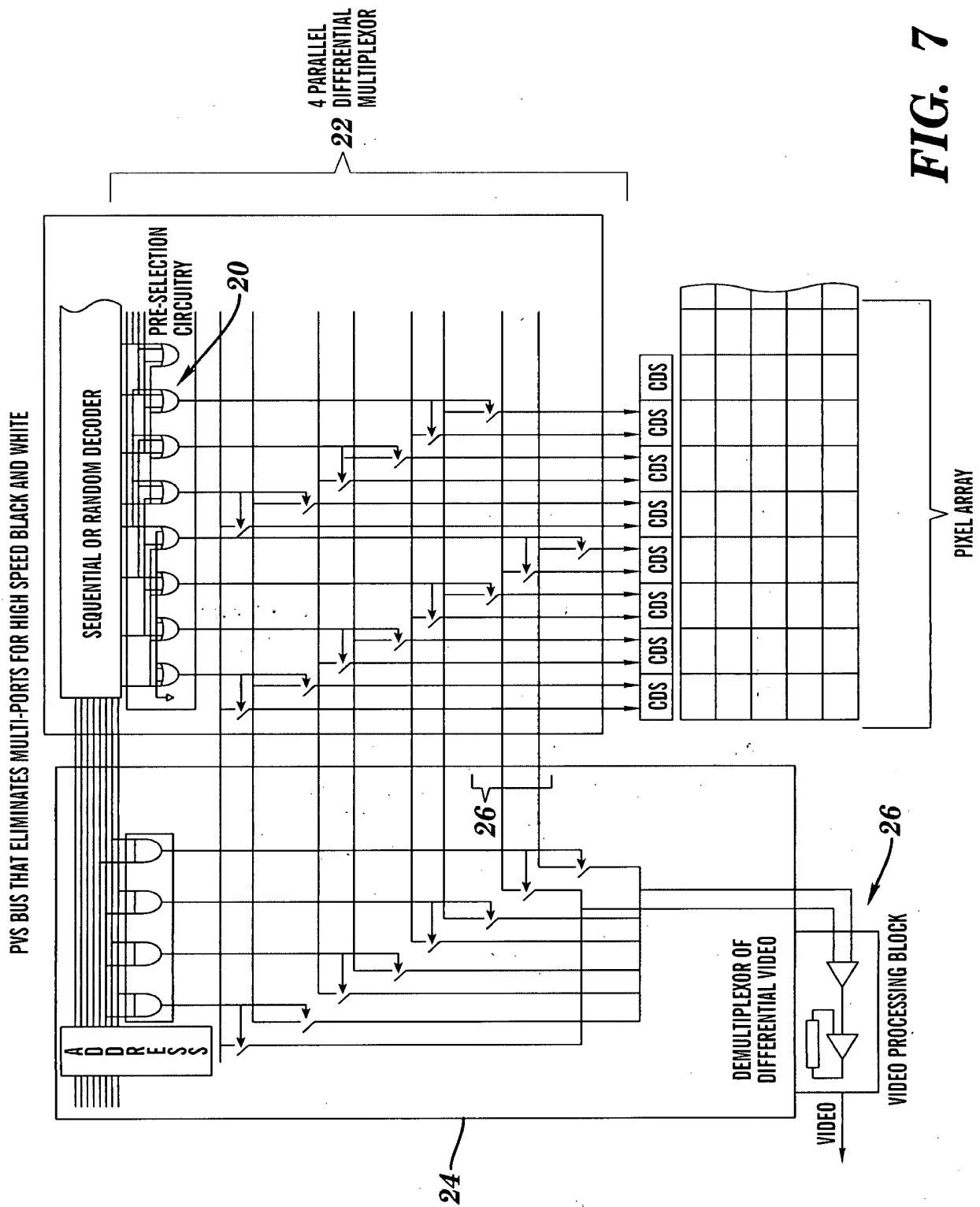
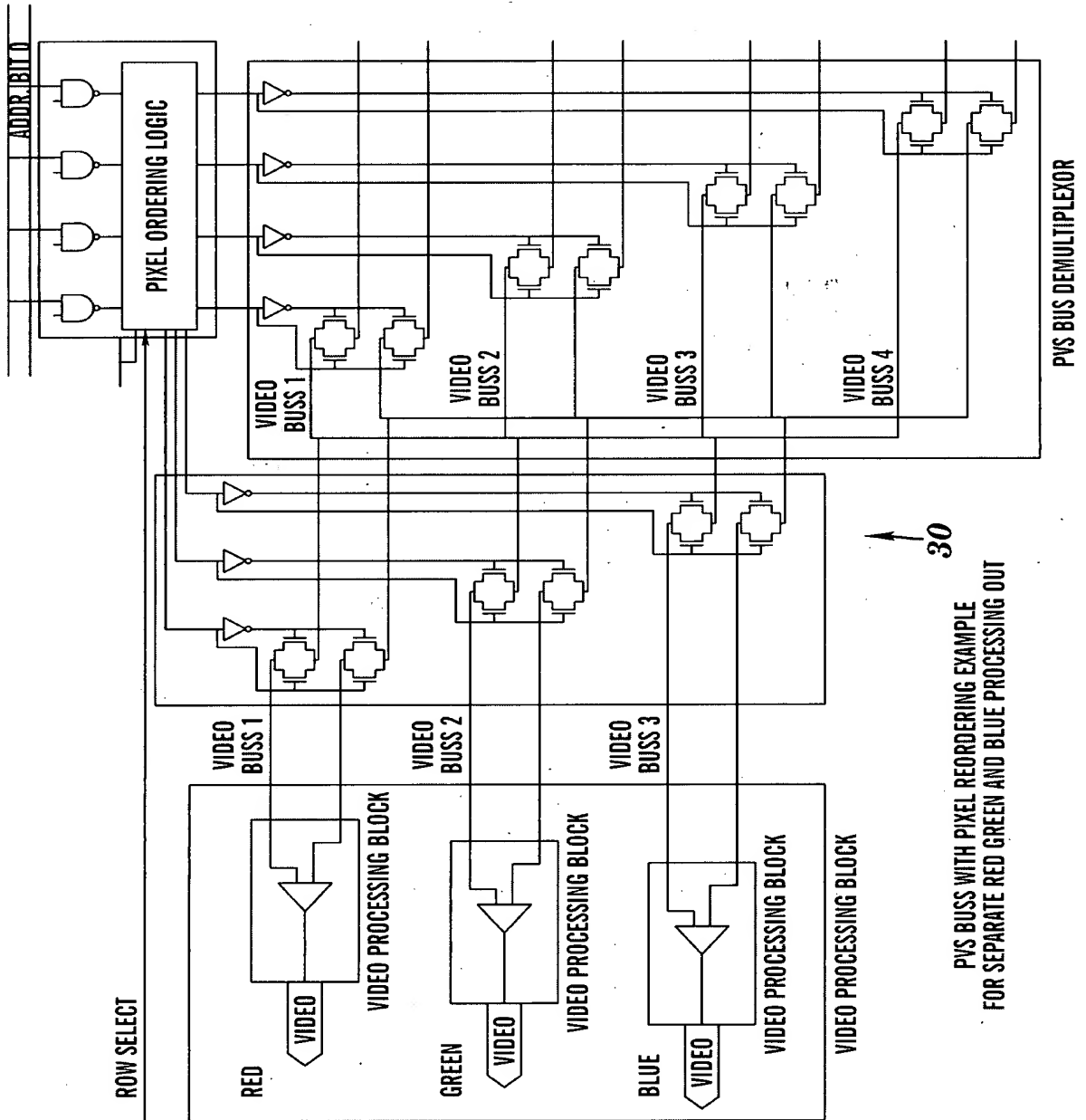


FIG. 6





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PVS BUSS WITH PIXEL REORDERING EXAMPLE
FOR SEPARATE RED GREEN AND BLUE PROCESSING OUT

FIG. 8

FIG. 9.

PVS BUS THAT ELIMINATES MULTI-PORTS FOR HIGH SPEED BLACK AND WHITE

The diagram illustrates a video processing system architecture. At the top, an **ADDRESS** input is connected to a **SEQUENTIAL OR RANDOM DECODER**. This decoder is linked to **PRE-SELECTION CIRCUITRY (20)**, which consists of a series of AND gates. The output of the pre-selection circuitry is connected to a **4 PARALLEL DIFFERENTIAL MULTIPLEXOR (22)**. This multiplexor is connected to a **DEMULTIPLEXOR OF DIFFERENTIAL VIDEO**. The output of the demultiplexor is connected to a **VIDEO PROCESSING BLOCK (26)**, which produces the final **VIDEO** output. The central part of the diagram is a grid of switches controlled by the bus. The output is a **VIDEO** signal.